AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claim 13 without prejudice. Please add new claims 14-19.

1. (CURRENTLY AMENDED) A system comprising:

a first circuit configured ~~to convert~~ for converting between ~~(i)~~ a differential serial signal ~~on a first differential interface~~ and ~~(ii)~~ a parallel signal, wherein said converting is one of (i) from said differential serial signal to said parallel signal and (ii) from said parallel signal to said differential serial signal;

a pair of non-crossing conductive paths carrying said differential serial signal between said first circuit and a differential interface connectable to a differential serial bus ~~connecting said first differential interface with a second differential interface~~; and

a second circuit (i) connected to said first circuit and (ii) configured to invert said parallel signal in response to a control signal in an inverting state.

2. (CURRENTLY AMENDED) The system according to claim 1, wherein ~~inverting said parallel signal is independently inverting~~

said second circuit is further configured to independently invert each bit of said parallel signal.

3. (ORIGINAL) The system according to claim 1, wherein said second circuit is further configured to buffer said parallel signal in response to said control signal in a non-inverting state.

4. (ORIGINAL) The system according to claim 1, wherein said second circuit comprises:

a plurality of inverters configured to invert each bit of said parallel signal to present an inverted parallel signal; and

a multiplexer configured to select between said parallel signal and said inverted parallel signal in response to said control signal.

5. (ORIGINAL) The system according to claim 1, wherein said second circuit comprises a plurality of exclusive-OR gates each configured to receive (i) one bit of said parallel signal and (ii) said control signal.

6. (ORIGINAL) The system according to claim 1, wherein said second circuit comprises (i) a pass gate and (ii) a tri-state inverter for each bit of said parallel signal.

7. (CURRENTLY AMENDED) A method of communicating on a differential serial bus, the method comprising the steps of:

(A) converting between a differential serial signal at a first differential interface and a parallel signal, wherein said converting is one of (i) from said differential serial signal to said parallel signal and (ii) from said parallel signal to said differential serial signal;

(B) routing said differential serial signal on non-crossing paths between said first differential interface and a second differential interface connectable to said differential serial bus ~~on non-crossing paths~~; and

(C) inverting said parallel signal in response to a control signal in an inverting state.

8. (CURRENTLY AMENDED) The method according to claim 7, wherein said inverting said parallel signal ~~is~~ comprises the sub-steps of independently inverting each bit of said parallel signal.

9. (ORIGINAL) The method according to claim 7, further comprising the step of buffering said parallel signal in response to said control signal in a non-inverting state.

10. (ORIGINAL) The method according to claim 7, wherein step (C) comprises the sub-steps of:

inverting said parallel signal to present an inverted parallel signal; and

multiplexing said parallel signal and said inverted parallel signal in response to said control signal.

11. (ORIGINAL) The method according to claim 7, wherein step (C) comprises the sub-step of logically exclusive-OR'ing each bit of said parallel signal with said control signal.

12. (ORIGINAL) The method according to claim 7, wherein step (C) comprises the sub-step of opening a pass gate and activating a tri-state inverter for each bit of said parallel signal in response to said control signal in said inverting state.

13. (CANCELED)

14. (NEW) A system comprising:

a transceiver circuit configured for converting between a first differential serial signal and a first parallel signal, wherein said converting is one of (i) from said first differential serial signal to said first parallel signal and (ii) from said first parallel signal to said first differential serial signal;

a first inverter circuit (i) connected to said transceiver circuit and (ii) configured to invert said first

differential serial signal in response to a first control signal in an inverting state; and

a pair of non-crossing conductive paths carrying said first differential serial signal between said first inverter circuit and a differential interface connectable to a differential serial bus.

15. (NEW) The system according to claim 14, wherein said transceiver circuit is further configured to convert between a second differential serial signal and a second parallel signal in an opposite direction than between said first differential signal and said first parallel signal.

16. (NEW) The system according to claim 15, further comprising a second inverter circuit (i) connected to said transceiver circuit and (ii) configured to invert said second differential serial signal in response to a second control signal in said inverting state.

17. (NEW) A method of communicating on a differential serial bus, the method comprising the steps of;

(A) converting between a first differential serial signal and a first parallel signal, wherein said converting is one of (i) from said first differential serial signal to said first

parallel signal and (ii) from said first parallel signal to said first differential serial signal;

(B) inverting said first differential signal at a first differential interface in response to a first control signal in an inverting state; and

(C) routing said first differential serial signal on first non-crossing paths between said first differential interface and a second differential interface connectable to said differential serial bus.

18. (NEW) The method according to claim 17, further comprising the step of routing a second differential serial signal from said second differential interface to a third differential serial interface on a second pair of non-crossing paths.

19. (NEW) The method according to claim 18, further comprising the steps of:

inverting said second differential serial signal at said third differential interface in response to a second command signal in said inverting state; and

converting said second differential serial signal to a second parallel signal after said inverting said second differential serial signal.